Amendments to the Specification

Please replace paragraph **[0002]** with the following amended paragraph:

[0002] This application is related to U.S. Application No. ~~(Atty Docket No. CPAC 1029-2)~~ 10/681,572, titled "Semiconductor stacked multi-package module having inverted second package"; U.S. Application No. ~~(Atty Docket No. CPAC 1029-3)~~ 10/681,735, titled "Semiconductor multi-package module having inverted land grid array (LGA) package stacked over ball grid array (BGA) package"; U.S. Application No. ~~(Atty Docket No. CPAC 1029-4)~~ 10/681,833, titled "Semiconductor stacked multi-package module having inverted second package and electrically shielded first package" U.S. Application No. ~~(Atty Docket No. CPAC 1029-5)~~ 10/681,583, titled "Semiconductor multi-package module having inverted second package stacked over die-down flip-chip ball grid array (BGA) package"; U.S. Application No. ~~(Atty Docket No. CPAC 1029-7)~~ 10/681,584, titled "Semiconductor multi-package module having inverted second package and including additional die or stacked package on second package"; U.S. Application No. ~~(Atty Docket No. CPAC 1029-8)~~ 10/681,734, titled "Semiconductor multi-package module having inverted bump chip carrier second package"; all filed 8 October 2003, and each of which is hereby incorporated by reference.

Please replace paragraph [0018] with the following amended paragraph:

[0018] Fig. **1B** is a diagrammatic sketch in a sectional view illustrating the structure of a BGA, generally similar to the BGA **11** shown in Fig. **1A**, except that here the molding **117** completely covers the substrate as well as the die and wire bonds. The molding configuration of Fig. **1B** is formed by applying the molding compound over an array of a number of BGAs, curing the molding, and then separating the encapsulated packages, for example by saw singulation. Typically the molding in such a package has vertical walls at the edges of the package. In such a package, unlike a BGA as in Fig. **1A**, no marginal portion of the upper surface of the substrate **12** is exposed and, accordingly, no electrical traces are exposed on the upper surface of the substrate. Many smaller packages currently are saw-singulated packages, often referred to as "chip scale packages."

Please replace paragraph [0025] with the following amended paragraph:

[0025] FIG. **4** is a diagrammatic sketch in a sectional view illustrating the structure of an example of a known 2-stack folded flexible substrate MPM, shown generally at **40**. The bottom package in the configuration of FIG. **4** has a 2-metal layer flexible substrate onto which the die is bonded via small beams to the first metal layer of the substrate. The second metal layer of the bottom package substrate carries the solder balls for connection to the underlying circuitry, such as a motherboard (not shown). The substrate is large enough to be folded over the top of the package, thus bringing the electrical interconnect lines upward where they are available for connection to the top package (an example of which is described below) by way of an array of solder balls on the top package. The space around the die and between the die and folded-over substrate is encapsulated **47** to provide protection and rigidity.

Please replace paragraph [00165] with the following amended paragraph:

[00165] Particularly, referring to FIG. **8B**, the bottom BGA package **300** of multipackage module **82** is provided with a metallic (for example, copper) heat spreader that surrounds the die and acts additionally as an electrical shield to electrically contain any electromagnetic radiation from the die in the lower BGA and thereby prevent interference with the die in the upper package. A lower planar part [[**354**]] **304** of the heat spreader is supported on the substrate **342** by legs or sidewalls [[**355**]] **305**. Spots or lines [[**356**]] **306** of an adhesive serve to affix the heat spreader supports [[**355**]] **305** to the lower surface of the bottom package substrate. The adhesive can be a conductive adhesive, and can be electrically connected to the lower metal layer **353** of the substrate **342**, particularly to a ground plane of the circuit and thereby establishing the heat spreader as an electrical shield. Or, the adhesive can be non-conductive and in such a configuration the heat spreader acts only as a heat spreading device. Alternatively, the shield enclosing the upward-facing bottom package die can be soldered or affixed using adhesive to the printed circuit board (or other installation surface for the module) at the time the solder balls are re-flowed to make the connection during installation of the module. Such an arrangement can provide an additional path for heat transfer, and can additionally provide electrical connection of the shield to the installation board, as may be desired for some applications. The supporting parts [[**355**]] **305** and the [[top part **354**]] lower planar part **304** of the heat spreader enclose the

die **344**, and can serve for protection from ambient and from mechanical stress to facilitate handling operations and, particularly, during subsequent testing before the MPM assembly.

Please replace paragraph [00177] with the following amended paragraph:

[00177] Inasmuch as no part of the upper surface of the bottom package substrate in the die-up configuration is occupied by the bottom package die, a plurality of top packages can be stacked over a plurality of package attach regions on the bottom package upper surface. This is illustrated by way of example in FIG. **8D**. FIG. **8D** is a diagrammatic sketch in a sectional view thru an embodiment of a multipackage module generally at [[**84**]] **86**, having a processor unit affixed to the lower surface of the bottom package generally as shown in FIG. **8A** (flip chip mounted in a "die-up" configuration), and a plurality of inverted LGA packages affixed to the upper side of the bottom package substrate according to an aspect of the invention.

Please replace paragraph [00180] with the following amended paragraph:

[00180] According to the invention, either the top package or the bottom package, or both of them, in the multi-package module of the invention can include two or more stacked chips. FIGS. **9A** and **9B** illustrate, by way of example, embodiments of the invention **90, 92** in which each of the lower BGA package **490** and the inverted upper LGA package **590** has two stacked die. The stacked die in each package in this example are wire-bonded to their respective substrates, and adjacent die are separated by a spacer, as is well known in the stacked-die package art. As will be appreciated, packages having other stacked die configurations, including other die interconnects, can be used in multi-package modules according to the invention, as well as side-by-side plural die arrangements. Referring particularly to FIG. **9A**, the bottom package **490** has stacked die **492** and **494** separated by a spacer **493**; and the inverted top package **590** has stacked die **592** and **594** separated by a spacer **593**. The z-interconnection between the top and bottom packages is formed by wire bonds **598**, connecting (in either forward- or reverse-bonding fashion) the upward-facing surfaces of the top and bottom package substrates. The inverted top package **590** is affixed onto the bottom package **490** using an adhesive **595**. A module encapsulation **907** encloses parts of the module above the bottom package substrate.